**WHAT IS CLAIMED IS:**

1. An apparatus capable of processing a multimedia digital bitstream, said apparatus comprising:

a processing chain comprising a plurality of media processors wherein each of said plurality of media processors is capable of processing a portion of said multimedia digital bitstream

wherein each of said plurality of media processors is capable of splitting said portion of said multimedia digital bitstream into a primary bitstream and a secondary bitstream, and capable of processing said primary bitstream, and capable of merging a processed primary bitstream with said secondary bitstream.

2. The apparatus as claimed in Claim 1 wherein the number of said plurality of media processors may vary from two to N, where N is an integer number greater than two.

3. The apparatus as claimed in Claim 1 wherein said multimedia digital bitstream comprises a high definition digital video signal.

4. The apparatus as claimed in Claim 1 wherein each of said plurality of media processors comprises a bitrate transcoder unit capable of transcoding a portion of said multimedia digital bitstream.

5. The apparatus as claimed in Claim 4 wherein said bitrate transcoder unit comprises a split unit, a BRT' transcoder, and a merge unit.

6. The apparatus as claimed in Claim 4 wherein said bitrate transcoder unit comprises an output component that is capable of generating empty data packets and adding said empty data packets to the output of said bitrate transcoder unit.

7. The apparatus as claimed in Claim 6 further comprising a clock control circuit in an output component of a last bitrate transcoder unit that is located at an output end of said processing chain, wherein said clock control circuit is capable of adjusting a clock rate of an output of said last bitrate transcoder unit in said processing chain.

8. The apparatus as claimed in Claim 1 wherein said processing chain further comprises:

an input block coupled to a first media processor in said processing chain, wherein said input block is capable of receiving multimedia data in real time from one of: a computer file, a bitpump, and a radio frequency front end; and

an output block coupled to a last media processor in said processing chain, wherein said output block is capable of outputting multimedia data in real time in one of: a computer file format, and a transport stream format.

9. A television unit comprising an apparatus capable of processing a multimedia digital bitstream, said apparatus comprising:

a processing chain comprising a plurality of media processors wherein each of said plurality of media processors is capable of processing a portion of said multimedia digital bitstream

wherein each of said plurality of media processors is capable of splitting said portion of said multimedia digital bitstream into a primary bitstream and a secondary bitstream, and capable of processing said primary bitstream, and capable of merging a processed primary bitstream with said secondary bitstream.

10. The television unit as claimed in Claim 9 wherein the number of said plurality of media processors may vary from two to N, where N is an integer number greater than two.

11. The television unit as claimed in Claim 9 wherein said multimedia digital bitstream comprises a high definition digital video signal.

12. The television unit as claimed in Claim 9 wherein each of said plurality of media processors comprises a bitrate transcoder unit capable of transcoding a portion of said multimedia digital bitstream.

13. The television unit as claimed in Claim 12 wherein said bitrate transcoder unit comprises a split unit, a BRT' transcoder, and a merge unit.

14. The television unit as claimed in Claim 12 wherein said bitrate transcoder unit comprises an output component that is capable of generating empty data packets and adding said empty data packets to the output of said bitrate transcoder unit.

15. The television unit as claimed in Claim 14 further comprising a clock control circuit in an output component of a last bitrate transcoder unit that is located at an output end of said processing chain, wherein said clock control circuit is capable of adjusting a clock rate of an output of said last bitrate transcoder unit in said processing chain.

16. The television unit as claimed in Claim 9 wherein said processing chain further comprises:

an input block coupled to a first media processor in said processing chain, wherein said input block is capable of receiving multimedia data in real time from one of: a computer file, a bitpump, and a radio frequency front end; and

an output block coupled to a last media processor in said processing chain, wherein said output block is capable of outputting multimedia data in real time in one of: a computer file format, and a transport stream format.

17. A method for processing a multimedia digital bitstream comprising the steps of:

processing a portion of said multimedia digital bitstream in each of a plurality of media processors of a processing chain;

wherein each of said plurality of media processors executes the steps of:

splitting said portion of said multimedia digital bitstream into a primary bitstream and a secondary bitstream;

processing said primary bitstream; and

merging a processed primary bitstream with said secondary bitstream.

18. The method for processing a multimedia digital bitstream as claimed in Claim 14 wherein the step of processing said primary bitstream comprises the step of:

transcoding said primary bitstream in a bitrate transcoder unit.

19. The method for processing a multimedia digital bitstream as claimed in Claim 18 further comprising the steps of:

generating empty data packets in an output component of said bitrate transcoder unit; and

adding said empty data packets to the output of said bitrate transcoder unit.

20. The method for processing a multimedia digital bitstream as claimed in Claim 19 further comprising the step of:

adjusting a clock rate of an output of at least one bitrate transcoder unit in said processing chain with a clock control circuit.